IN THE CLAIMS

Please amend the claims as follows:

1. (Currently Amended) A method comprising:

receiving in an Ingrained Sharing Directory Cache (ISDC) an incoming operation request including an associated incoming memory address;

locating pending operation in the ISDC pending queue;

completing a pending ISDC entry if the incoming operation is an ISDS data reply~~;~~;

performing the operation, if there is an ISDC entry associated with the incoming memory address~~;~~; and

creating an ISDC entry if there is no ISDC entry associated with the incoming operation request~~;~~, wherein creation includes,

requesting information associated with the incoming memory address, wherein the information is requested from an Ingrained Sharing Directory Storage (ISDS)~~;~~;

evicting another ISDC entry if there is no free ISDC entry~~;~~, wherein the eviction includes,

requesting the ISDS to store the information evicted from the other ISDC entry~~;~~; and

designating the evicted ISDC entry to the incoming request, and marking the evicted ISDC entry as pending; and

storing the incoming request into the ISDC pending queue.

2. (Original) The method of claim 1, wherein the ISDC entry associated with an incoming memory address indicates whether one or more cached copies of a memory line are in shared or dirty-exclusive state.

3. (Currently Amended) A method comprising:

receiving an Ingrained Sharing Directory Storage (ISDS) request; and

selecting an entry in an ISDS, wherein the ISDS includes,

a plurality of coherence buffers, wherein each set of the coherence buffers maintains a dynamic full map of memory lines cached in a given set in system caches and evicted from an ISDC, wherein each of the coherence buffers maintains a plurality of cells, wherein each of the cells maintains a dynamic full map of shared lines cached in a given set of a given system cache and evicted from the ISDC, and wherein each of the cells maintains a plurality of entries, each of the entries comprising a memory address of an associated memory line.

4. (Currently Amended) The method of claim 3, wherein the selecting includes,

selecting one of the coherence buffers based on a SELECT_CB field of an incoming address of an ISDS request; ~~and~~

selecting one of the cells in the selected coherence buffer based on a SELECT_CELL field of an incoming address of an ISDS request, wherein value of the SELECT_CELL field is associated with one of plurality system caches; and

using a MEMORY_TAG field of the incoming address or the VALID field or the eviction policy to select an ISDS entry.

5. (Original) The method of claim 4, wherein the ISDS request stores the MEMORY_TAG field and a state of the memory line into the one or more of ISDS entries.

6. (Original) The method of claim 3, wherein information about copies of a given memory line resides in only one of the coherence buffers.

7. (Original) An Ingrained Sharing Directory (ISD) controller apparatus for maintaining coherence of cache lines in a multi-cache system, wherein the ISD controller maintains a dynamic full map directory of local memory lines cached in the system caches, and wherein the ISD controller comprises:

an Ingrained Sharing Directory Cache (ISDC) to store information about memory lines recently cached in the system caches;

an Ingrained Sharing Directory Storage (ISDS) to store information about memory lines evicted from an ISDC; and

an ISDC pending queue to store pending ISDC operations.

8. (Original) The apparatus of claim 7 wherein the ISDC set and the ISDS set combined include all copies of memory lines cached at any point in time in the system caches.

9. (Original) The apparatus of claim 7, wherein the each of system caches is a set-associative cache.

10. (Original) An apparatus comprising:

an Ingrained Sharing Directory Cache (ISDC) to store state information about recent copies of local memory blocks, the ISDC to receive Ingrained Sharing Directory Storage (ISDS) requests and create ISDC entries from information presented by the ISDS; and

an ISDC pending queue to store pending ISDC operations.

11. (Original) The apparatus of claim 10, wherein the state information indicates whether the copy of local memory line is dirty exclusive or shared.

12. (Original) The apparatus of claim 10, wherein the ISDC requests are requests to fetch or modify the state information about the copy of the local memory line.

13. (Original) A system for maintaining coherence of cache lines in multi-cache system comprising:

a system interconnect; and

a first number of nodes connected via the system interconnect, wherein each of the nodes includes a local memory unit to store local data, wherein each local memory unit includes a plurality of memory lines, and wherein each node includes,

a second number of local set-associative system caches, and wherein each of the local caches comprise a third number of cache sets, and wherein each of the sets comprise a fourth number of cache lines;

a local ISD controller, wherein the local ISD controller comprises,

an Ingrained Sharing DirectoryCache (ISDC) to store state information about the recent copies of the local data;

an Ingrained Sharing Directory Storage (ISDS) to store information evicted from the ISDC, wherein the ISDS includes a fifth number of coherence buffers, wherein each of the coherence buffers contains a sixth number of cells, wherein each of the cells contains a seventh number of ISDS entries and wherein an eight number of ISDS entries is equal to the product of the first number of nodes, the second number of local set-associative system caches, the third number of cache sets, and the fourth number of cache lines; and

an ISDC pending queue to store pending ISDC operations.

14. (Original) The system of claim 13, wherein the fifth number of coherence buffers is equal to the third number of cache sets.

15. (Original) The system of claim 13, wherein the sixth number of cells is equal to the product of the first number of nodes and the second number of local set-associative system caches.

16. (Original) The system of claim 13, wherein the seventh number of ISDS entries is equal to the fourth number of cache lines.

17. (Original) The system of claim 13, wherein the memory unit includes random access memory

18. (New) A method comprising:

receiving in an Ingrained Sharing Directory Cache (ISDC) an operation request associated with a memory address;

determining whether a first ISDC entry associated with the memory address is in the ISDC;

creating the first ISDC entry, if the first ISDC entry is not in the ISDC, wherein the creating includes,

receiving information associated with the memory address from an Ingrained Sharing Directory Storage (ISDS);

determining if there is a free ISDC entry in the ISDC;

evicting a second ISDC entry, if the free ISDC entry is not in the ISDC, wherein the evicting includes,

sending information stored in the second ISDC entry to the ISDS; and

designating the second ISDC entry as the free ISDC entry; and

replacing the free ISDC entry with the first ISDC entry; and

performing the operation request using the first ISDC entry.

19. (New) The method of claim 18 wherein the evicting further includes marking the first ISDC entry pending.

20. (New) The method of claim 19 further comprising completing a pending ISDC entry if the operation request type is a data reply.

21. (New) The method of claim 18, wherein the information associated with the memory address indicates whether a system cache copy of a memory line unit is the only copy of the memory line in the system, wherein the memory line is located at the memory address.

22. (New) A method comprising:

receiving an ISDS entry request associated with an ISDS entry; and

selecting the ISDS entry from an ISDS, wherein the ISDS includes a first set of coherence buffers, wherein each of the first set of coherence buffers includes,

a second set of coherence buffer cells, wherein each of the second set of coherence buffer cells is associated with one or more of a plurality of system caches; and

a third set of ISDS entries, wherein each of the

ISDS entries is adapted to store information about one of a fourth set of system cache copies of local memory lines, and wherein the third set of ISDS entries includes the ISDS entry.

23. (New) The method of claim 22, wherein the selecting includes,

selecting one of the first set of coherence buffers based on a local memory line address; and

using a system cache identifier to select one of the second set of coherence buffer cells, wherein the system cache identifier is associated with one of the plurality of system caches; and

using a memory tag field to select the ISDS entry.

24. (New) The method of claim 22, wherein the ISDS entry request specifies the system cache identifier and a request type.

25. (New) The method of claim 22, wherein information about copies of one memory line reside in only one of the first set of coherence buffers.

26. (New) An apparatus comprising:

an Ingrained Sharing Directory Cache (ISDC) to store state information about a first set of memory lines of a memory unit, wherein copies of the first set of memory lines are stored in one or more system caches; and

an Ingrained Sharing Directory Storage (ISDS) to store state information about a second set of memory lines of the memory unit, wherein copies of the second set of memory lines are stored in one or more of the system caches, and wherein no memory line in the first set is in the second set.

27. (New) The apparatus of claim 26 wherein the first set and the second set combined include all copies of memory lines of the memory unit stored in one or more of the system caches.

28. (New) An apparatus comprising:
an ISDS to store state information about copies of local memory blocks, wherein the ISDS includes,
a first set of entries, wherein each entry can contain state information about a copy of a local memory line;
a second set of cells, wherein each of the cells includes ones of the first set of entries, and wherein each cell is associated with one of a third set of system caches; and
a fourth set of coherence buffers, wherein each of the coherence buffers includes ones of the second set of cells; and
an ISDC to receive ISDC requests and fetch the state information from the ISDS;

29. (New) The apparatus of claim 28, wherein the state information indicates whether the copies of local memory lines are dirty-exclusive.

30. (New) The apparatus of claim 28, wherein the each of the third set of system caches includes set-associative caches.

31. (New) The apparatus of claim 28, wherein the ISDC requests are requests to fetch or modify the state information about the copy of the local memory line.

32. (New) A system comprising:
a plurality of nodes, wherein the plurality of nodes includes a first number of set-associative caches, and wherein each node includes,
a memory unit to store local data, wherein the memory unit includes a second number of regions, and wherein each region includes a plurality of memory lines;

at least one of the first number of set-associative caches to store copies of the local data and data stored on others of the nodes, wherein the at least one set-associative cache includes a third number of sets, wherein the third number is equal to the second number, and wherein each set has a fourth number of cache lines;

an ISDC to store state information about copies of the local data; and

an ISDS to store state information about copies of the local data, wherein the cache coherence directory includes,

a fifth number of coherence buffers, wherein the fifth number of coherence buffers is equal to the third number of sets;

a sixth number of cells, wherein the sixth number of cells is equal to the first number of set-associative caches; and

a seventh number of directory entries, wherein the seventh number of directory entries is equal to the product of the first number of set-associative caches, the third number of sets, and the fourth number of cache lines.

33. (New) The system of claim 32, wherein the memory unit includes random access memory.

34. (New) The system of claim 32, wherein the set-associative caches are selected from a set consisting of 4-way set associative caches, 8-way set associative caches, and 16-way set associative caches.

35. (New) A machine-readable medium that provides instructions, which when executed by a machine, cause the machine to perform operations comprising:

receiving in an Ingrained Sharing Directory Cache (ISDC) an operation request associated with a memory address;

determining whether a first ISDC entry associated with the memory address is in the ISDC;

creating the first ISDC entry, if the first ISDC entry is not in the ISDC, wherein the creating includes,

receiving information associated with the memory address from an Ingrained Sharing Directory Storage (ISDS);

determining if there is a free ISDC entry in the ISDC;

evicting a second ISDC entry, if the free ISDC entry is not in the ISDC, wherein the evicting includes,

sending information stored in the second ISDC entry to the ISDS; and

designating the second ISDC entry as the free ISDC entry; and

replacing the free ISDC entry with the first ISDC entry; and

performing the operation request using the first ISDC entry.

36. (New) The machine-readable medium of claim 35, wherein the evicting further includes marking the first ISDC entry pending.

37. (New) The machine-readable medium of claim 36 further comprising completing a pending ISDC entry if the operation request type is a data reply.

38. (New) The machine-readable medium of claim 35, wherein the information associated with the memory address indicates whether a system cache copy of a memory line unit is the only copy of the memory line in the system, wherein the memory line is located at the memory address.

39. (New) A machine-readable medium that provides instructions, which when executed by a machine, cause the machine to perform operations comprising:

receiving an ISDS entry request associated with an ISDS entry; and

selecting the ISDS entry from an ISDS, wherein the ISDS includes,

a first set of coherence buffers, wherein each of the first set of coherence buffers includes,

a second set of coherence buffer cells, wherein each of the second set of coherence buffer cells is associated with one or more of a plurality of system caches, and

a third set of ISDS entries, wherein each of the ISDS entries is adapted to store information about one of a fourth set of system cache copies of local memory lines, and wherein the third set of ISDS entries includes the ISDS entry.

40. (New) The machine-readable medium of claim 39, wherein the selecting includes,

selecting one of the first set of coherence buffers based on a local memory line address;

using a system cache identifier to select one of the second set of coherence buffer cells, wherein the system cache identifier is associated with one of the plurality of system caches; and

using a memory tag field to select the ISDS entry.

41. (New) The machine-readable medium of claim 39, wherein the ISDS entry request specifies the system cache identifier and a request type.

42. (New) The machine-readable medium of claim 39, wherein information about copies of one memory line reside in only one of the first set of coherence buffers.